In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) A method for manufacturing buried connections in an integrated circuit, comprising:

providing a structure formed of a first support wafer glued onto a rear surface of a thin semiconductor wafer, one or several elements of the integrated circuit being ~~possibly~~ formed in and above the thin semiconductor wafer;

gluing a second support wafer on the structure on ~~the~~ a front surface side of the thin semiconductor wafer;

removing the first support wafer;

forming interconnections ~~connections~~ between opened ~~different~~ areas of the rear surface of the thin semiconductor wafer;

gluing a third support wafer on the interconnections ~~connections~~; and

removing the second support wafer.

2. (Currently Amended) The method of claim 1, wherein the step of providing the structure formed of the first support wafer glued onto a rear surface of the thin semiconductor wafer, further comprises:

gluing the thin semiconductor wafer and the first support wafer ~~are glued via~~ using ~~an~~ the insulating ~~wafer~~ layer.

3. (Currently Amended) The method of claim ~~1~~ 2, wherein the step of forming the interconnections ~~connections~~ comprises the steps of:

etching ~~openings~~ open areas in ~~an~~ the insulating layer ~~formed on the rear surface of the thin wafer~~; and

filling the ~~openings~~ open areas with a conductive material.

4. (Currently Amended) The method of claim 3, further comprising, after the step of etching ~~openings~~ open areas in the insulating layer, an ~~step of~~ etching ~~areas of~~ step to produce areas of reduced thickness in the insulating layer, the areas of reduced thickness being then filled ~~like said openings~~ with a conductive material.

5. (Currently Amended) The method of claim 3, wherein the filling of the ~~openings~~ open areas with a conductive material comprises:

depositing a metal layer on the structure on ~~the~~ a side of the insulating layer and of the ~~openings~~ open areas; and

annealing to form a silicide layer ~~at~~ in the ~~bottom of the openings~~ open areas.

6. (Currently Amended) The method of claim ~~3~~ 4, comprising, after the step of filling the ~~openings~~ open areas and ~~possibly~~ the areas of reduced thickness:

performing a chem-mech polishing of the conductive filling material to expose the insulating layer to obtain a planar surface; and

covering said planar surface with a second insulating layer; and

wherein the gluing the third support wafer on the interconnections is done using the second insulating layer.

7. (Original) The method of claim 1, comprising, prior to the gluing of the second support wafer, a step of covering the structure with a bonding layer.

8. (Withdrawn) An integrated circuit comprising components formed in and above a thin semiconductor wafer attached on a support wafer placed at the rear surface of the thin wafer, the rear surface of the thin wafer being covered with a first insulating layer comprising openings crossing the thin wafer, the openings containing conductive portions in contact with some areas of the rear surface of the thin semiconductor wafer, said conductive portions being made of silicide.

9. (Withdrawn) The integrated circuit of claim 8, wherein some of the said conductive portions are in contact with conductive wells crossing the thin wafer, the conductive wells being eventually made of silicide.

10. (New) A method for manufacturing buried connections in an integrated circuit, comprising:

attaching a first support wafer to a first surface of a thin semiconductor wafer;

attaching a second support wafer to a second surface of the thin semiconductor wafer;

removing the first support wafer;

forming interconnections between opened areas of the first surface of the thin semiconductor wafer;

attaching a third support wafer to the interconnections; and

removing the second support wafer.

11. (New) The method of claim 10, wherein the method of attaching a first support wafer to a first surface of a thin semiconductor wafer, further comprises:

attaching the thin semiconductor wafer and the first support wafer using an insulating layer.

12. (New) The method of claim 11, wherein the step of forming the interconnections comprises the steps of:

etching open areas in the insulating layer; and

filling the open areas with a conductive material.

13. (New) The method of claim 12, wherein further comprising, after the step of etching open areas in the insulating layer, an etching step to produce areas of reduced thickness in the insulating layer, the areas of reduced thickness being then filled with a conductive material.

14. (New) The method of claim 13, wherein filling the open areas with a conductive material comprises:

depositing a metal layer on the structure on a side of the insulating layer and of the open areas; and

annealing to form a silicide layer in the open areas.

15. (New) The method of claim 13, comprising, after the step of filling the open areas and the areas of reduced thickness:

performing a chem-mech polishing of the conductive filling material to expose the insulating layer to obtain a planar surface; and

covering said planar surface with a second insulating layer; and

wherein the gluing the third support wafer on the interconnections is done using the second insulating layer.

16. The method of claim 10, comprising, prior to the gluing of the second support wafer, a step of covering the structure with a bonding layer.